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jc931 U.S. PTO 09/13/00

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	RCA 89,970
First Inventor or Application Identifier	Robert Warren Schmidt
Title	VOLTAGE LEVEL TRANSLATION CIRCUITS
Express Mail Label No.	EL479512753US

jc682 U.S. PTO 09/663156 09/13/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 7] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]
4. Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEM 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: _____

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____
    Prior application information: Examiner _____ Group / Art Unit: _____
    For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

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Name (Print/Type)	Frederick A. Wein	Registration No. (Attorney/Agent)	27,168
Signature		Date	9/13/00

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TOTAL AMOUNT OF PAYMENT ($) 690.00

Complete if Known	
Application Number	
Filing Date	Herewith
First Named Inventor	Robert Warren Schmidt
Examiner Name	
Group / Art Unit	
Attorney Docket No.	RCA 89,970

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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Deposit Account Name: THOMSON multimedia Licensing Inc.

☒ Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. ☐ **Payment Enclosed:** ☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	690.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims	1 - 20** =	0	X	0	= 0
Independent Claims	1 - 3** =	0	X	0	= 0
Multiple Dependent				0	= 0

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	890	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	
				Other fee (specify) _____	
				Other fee (specify) _____	

* Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 0

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Frederick A. Wein	Registration No. (Attorney/Agent)	27,168	Telephone	609-734-9518
Signature				Date	9/13/00

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VOLTAGE LEVEL TRANSLATION CIRCUITS

CLAIM OF PRIORITY

Priority is claimed from U.S. Provisional Application No. 60/174,695 filed January 6, 2000.

TECHNICAL FIELD

The present invention relates to the field of the operation of integrated circuits; and more particularly, relates to the adaptation of integrated circuits to work with power supplies having incompatible configurations and/or voltage levels. In both cases, the incompatibility is overcome by using voltage level translation.

BACKGROUND

In consumer electronics where low cost is an important engineering parameter, it is not uncommon to design using low cost parts in a manner in which the part was not designed to be used. Such a case can be where the power supply for a device has been designed for other purposes and it becomes necessary to use this seemingly incompatible power supply for providing an auxiliary feature. Such a case can be for a DVD player where the power supply is a balanced split level power supply, i.e., ±5.0 volts with a center tapped ground, and it is desirable for cost reasons to use an integrated circuit which is designed for a single ended power supply with input and output coupling capacitors, which are desirable to eliminate. Such input and output coupling capacitors represent an extra parts cost and also can take up printed circuit board space which sometimes is very limited. Moreover, if the input and output capacitors are electrolytics, they are particularly larger than other capacitors and represent an additional reliability problem which is desirable to eliminate.

Additionally, the incompatibility of power supply and integrated circuit configurations can occur in, for example, a digital circuit system, where various subsystems operate with different power and voltage requirements. Some integrated circuit protocols and systems require a supply voltage with a Vcc (the positive rail voltage) of 3.3 volts and a Vss (the lower rail voltage) of ground potential, while others may require a Vcc -to-Vss voltage of 5.0 volts or 2.9 volts.

Still further concerning incompatible voltages available from a power supply, many integrated circuits are extremely sensitive to over-voltage or over-current, since

such overages can not only provide incorrect results (particularly if the integrated circuit is digital) but can also cause physical damage to the integrated circuit. Most processors have voltage and current ratings that may not be exceeded by even a little bit without causing severe damage to the integrated circuit. For example, it is not uncommon for microprocessors designed for operating at a power supply voltage of 3.3 volts to be damaged by application of signals in excess of a peak to peak of 3.45 volts when reading data from RAMs in which the high/low voltage differential is 5.0 volts. Therefore, closely limiting the voltage supply levels to meet specification is essential to the operation of integrated circuits.

SUMMARY OF THE INVENTION

A first embodiment of a voltage level translator is presented for operating an operational amplifier integrated circuit designed for operation with a single ended power supply, to operate with a split level power supply having a center tapped ground. A first polarity power supply terminal of a operational amplifier integrated circuit is connected to a first polarity of the of the split level power supply, and a second polarity power supply terminal of the operational amplifier integrated circuit is connected to an second polarity of the power supply, with a signal input terminal of the operational amplifier being connected to the center tapped ground.

A second embodiment of a voltage level translator is presented to permit an integrated circuit having a predetermined maximum voltage rating to be operated with a split level power supply having a power supply voltage greater than the voltage rating, wherein a first voltage translation zener diode is coupled in series between a first polarity of the power supply and an appropriate first polarity terminal of the integrated circuit, and a second voltage translation zener diode is coupled in series between a second polarity of the power supply and an second polarity terminal of the integrated circuit,

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial schematic,-partial block diagram of a prior art circuit.

Fig. 2 is a schematic of the amplifier of Fig. 1 incorporating the two translation circuits according to aspects of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Fig. 1 is a prior art partial schematic,-partial block diagram of an applications circuit for an LM4881 integrated circuit, as recommended by the manufacturer of the integrated circuit, ©1997 National Semiconductor Corporation USA., and appropriately modified to comply with patent application requirements.

Referring to Fig. 1, an amplifier system, generally designated 10, includes an integrated circuit chip 12, which, in the exemplary embodiment, provides a pair of operational amplifiers 14R, 14L for respective L and R stereophonic amplification and sound reproduction. Signals R and L are coupled to inverting inputs 17R, 17L of respective amplifiers 14R, 14L through respective coupling capacitors 18R, 18L and isolation resistors 20R, 20L. Output signals of amplifiers 14R, 14L at terminals 15R, 15L, drive respective loudspeakers 16R, 16L through coupling capacitors 22R, 22L. Loudspeakers 16R, 16L in the present case are earphone speakers.

Power for this arrangement is provided by a single ended power supply (not shown), with one side grounded at node 24, and positive voltage V_{DD} provided at node 26. Resistors 28R, 28L form a divider for providing a virtual AC reference signal ground at their junction for non-inverting terminals 30R, 30L through coupling capacitor 32. Power supply decoupling capacitor 33 prevents high frequency common mode feedback through the power supply. Resistors 36R, 36L in parallel with respective high frequency roll-off capacitors 38R, 38L, from respective output terminals 15R, 15L, to inverting terminals 17R, 17L and isolation resistors 20r, 20L, provide negative signal feedback and prevent oscillation with a high frequency roll-off. Resistors 40R, 40L provide a DC return for leakage currents thus improving DC stability. Shut-down circuit 41 is internal to integrated circuit 12.

Particular note should be made of DC blocking, coupling capacitors 18R, 18L, 22R, 22L as well as AC ground coupling capacitor 32. By the voltage translation disclosed in connection with Fig. 2 of the circuit of Fig. 1, so that the circuit is powered by a split voltage power supply with a center tapped ground, these five coupling capacitors are eliminated, as will be discussed below.

The single-ended power supply used for Fig. 1 (not shown) and the split voltage power supply with a center tapped ground (not shown) used for Fig. 2, are both well known power supply configurations which can be found, inter alia, in the Motorola™ Silicon Rectifier Handbook, ©1966, at pages 4-10 and 6-4 respectively. The single ended power supply can be a full wave or full wave bridge power supply with a single

DC polarity to ground. The "split voltage power supply" is commonly referred to as a full wave bridge doubler, generating opposite DC polarities with respect to an AC input lead which serves as ground. The ground serves as a center tapped AC ground return at the junction of series power supply capacitors, as well as a DC ground for the plus and minus DC power supply voltages.

The device into which the described headphone amplifier is to be installed, is a DVD player. One of the "incompatibility" problems is that the configuration of the DVD power supply is a "split voltage power supply" which is not compatible with the integrated circuit, which was designed for a single ended power supply, as discussed in Fig. 1. The second of the "incompatibility" problems is that once the configuration incompatibility problem is overcome, the power supply voltages of the second power supply exceeded the maximum voltage specifications for the chosen integrated circuit. Both problems of "incompatibility" are overcome by the voltage translation circuits shown in Fig. 2, and discussed and claimed below, wherein like members to the members of Fig. 1 are given like numeral designations.

Referring now to Fig. 2, the circuit of Fig. 1 is voltage translated to be used with a split voltage power supply having plus and minus voltages available with a center tapped ground, wherein node 26 is connected to the plus voltage supply, node 24 is connected to the negative voltage supply and ground node 40 is connected to the center tapped ground. In this way, the voltages of the integrated circuit are translated negative by one half the total voltage of the single ended supply of Fig. 1.

Since the ground terminal is now an actual ground voltage of the split level power supply instead of a virtual ground for the single ended power supply as provided by divider resistors 28R, 28L and capacitor 32, the DC blocking capacitors 18R, 18L, 22R and 22L are no longer required because the AC ground is at the power supply voltage of DC ground. Since the AC and DC grounds are now at the same DC voltage, capacitor 32 also becomes unnecessary.

Having solved the configuration "incompatibility" problem and saved five coupling capacitors by voltage translation, this leaves the voltage level "incompatibility" problem. The present invention also discloses a system comprising a level translator circuit having level translators provided by a zener diode conducting in the zener region, with each zener diode reducing the voltage level on one side of the split level power supply applied to integrated circuit 12. The translation of voltages from a first voltage level to a second voltage level is provided by generating a zener voltage and

applying the zener voltage as a voltage drop between the power supply terminals and the operational amplifier nodes 24, 26.

In the present instance, the split level power supply voltages are ±5.0 volts but the particular integrated circuit is specified for 5.5 volts maximum. This 10 volt supply exceeds the maximum voltage rating of the integrated circuit since it is possible that adjacent parts of the integrated circuit may have a 10 volt differential between them, e.g., if the integrated circuit chip substrate is internally connected to one of the power supply voltages and not to ground.

This possible over-voltage condition is solved by adding two 2.4 volt zener diodes 50, 52 poled in their zener polarity, each added in series with one side of the split power supply voltages. The two zener diodes thus provide a 2 x 2.4 = 4.8 volt drop to bring the maximum power supply voltage to 5.2 volts across the integrated circuit 12. Thus, each of the split voltage power supply sides of ±5.0 volts are translated downward to ±2.6 volts. Zener diodes 50, 52 are selected to be in the zener region of their characteristic at the DC current drawn by the amplifiers 14R, 14L. In the alternative, non-zener silicon diodes, poled in the forward conducting direction, can also be used (not shown), e.g. four diodes each having a 0.6 voltage drop, would provide a 2.4 volts drop instead of a zener diode. The value of the zener voltages or the number of forward biased silicon diodes can be chosen according to the level of voltage drop desired. However, using zener diodes, provides better power supply regulation.

The present embodiment(s) shows the operational amplifiers 14R, 14L in an inverting amplifier configuration where the gain $A_v = R_f/R_i$ where R_f is the negative feedback resistor and R_i is the input impedance at terminal 17R, 17L. The present embodiments also apply with the operational amplifiers 14R, 14L connected in a non-inverting amplifier configuration (not shown), i.e., the feedback resistors are returned to the non-inverting terminals 30R, 30L with a gain $A_v = 1+(R_f/R_i)$ and the inverting terminals 17R, 17L are coupled to ground.

The present embodiment(s) show a voltage translation from an over-voltage power supply which is a split level power supply. It is within the contemplation of the present invention that a single ended over-voltage power supply can be used in which case only a single zener diode need be used.

CLAIMS

1. A voltage level translator for operating an operational amplifier integrated circuit designed for operation with a single ended power supply, to operate with a split level power supply having a center tapped ground, comprising:

first means for connecting a first polarity power supply terminal of the operational amplifier integrated circuit to a first polarity of the power supply,

second means for connecting a second polarity power supply terminal of the operational amplifier integrated circuit to a second polarity of the split level power supply, and

means for connecting a signal input terminal of the operational amplifier to a center tapped ground of the split level power supply.

2. The voltage level translator of claim 1 wherein another signal input terminal of the operational amplifier is coupled to a signal source referenced to ground without any DC isolation capacitors connected in series with the amplifier and the output terminal of the operational amplifier is coupled to a signal load referenced to ground without any DC isolation capacitors connected in series with the amplifier.

3. The voltage level translator of claim 2 wherein the signal load is a loudspeaker having one terminal referenced to ground.

4. The voltage level translator of claim 1 wherein the amplifier includes a plurality of amplifiers on the same integrated circuit chip having a common substrate, and all of the plurality of amplifiers are also voltage level translated, the substrate being biased the same amount with respect to each of the plurality of amplifiers.

5. The voltage level translator of claim 1 wherein the split level power supply having a center tapped ground also provides power to other circuits performing other functions.

6. The voltage level translator of claim 5 wherein the amplifier output load is an earphone and the other circuits performing other functions is a DVD player.

7. The voltage level translator of claim 1 wherein the amplifier has an AC reference which is connected to the DC voltage ground.

ABSTRACT

Voltage level translators are presented, inter alia, for operating an operational amplifier integrated circuit designed for operation with a single ended power supply, to operate with a split level power supply having a center tapped ground. A first polarity power supply terminal of a operational amplifier integrated circuit is coupled to a first polarity of the of the split level power supply, and a second polarity power supply terminal of the operational amplifier integrated circuit is coupled to a second polarity of the power supply, with a positive signal input terminal of the operational amplifier being coupled to a center tapped ground of the split level power supply. A second voltage level translator is presented to operate an integrated circuit having a maximum voltage rating with a power supply having a power supply voltage greater than the maximum voltage rating, wherein a first zener diode is coupled in series between a first polarity of the power supply and a first polarity terminal of the integrated circuit, and a second zener diode is coupled in series between a second polarity of the power supply and a second polarity terminal of the integrated circuit.

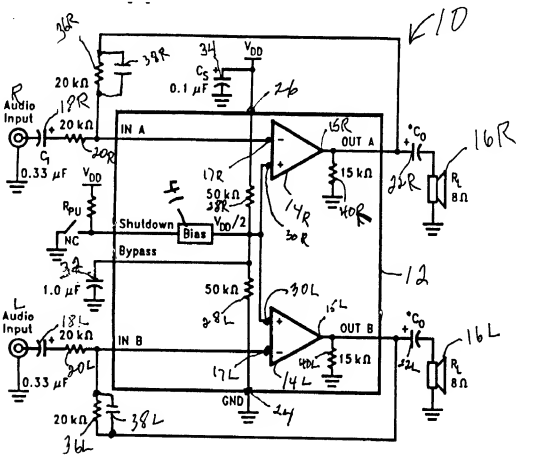
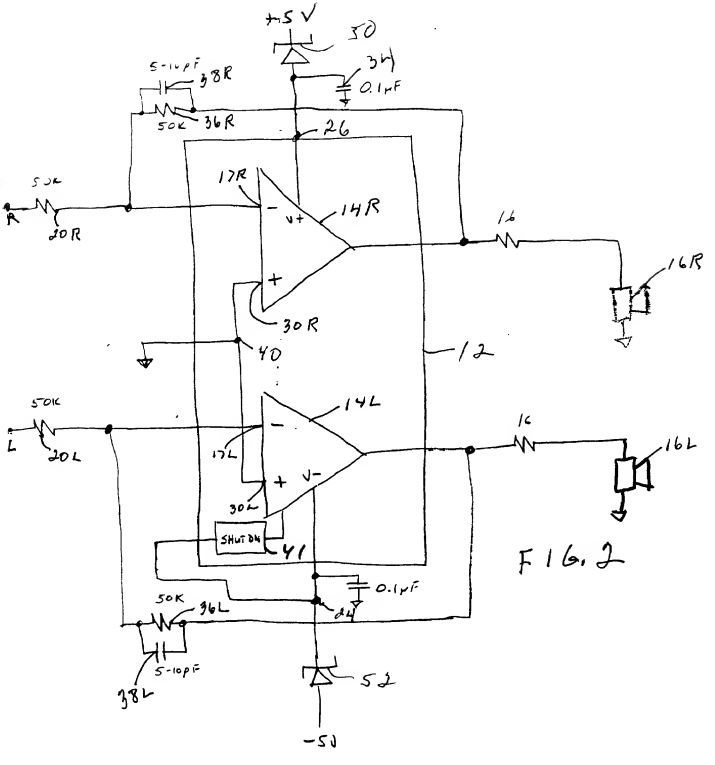


FIG. 1. PRIOR ART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50K
36R
26
17R
14R
V+
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R
20R
30R
40
12
50K
14L
L
20L
17L
V-
1K
16L
30K
SHUTDN
41
0.1μF
44
50K
36L
5-10pF
38L
52
-5V

FIG. 2